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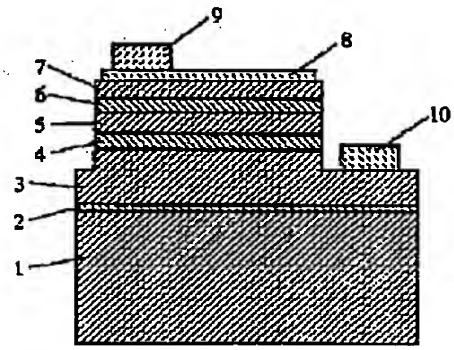
TITLE : NITRIDE SEMICONDUCTOR ELEMENT



ABSTRACT : PROBLEM TO BE SOLVED: To improve the output of an LED, LD by providing the structure of a new nitride semiconductor element.

SOLUTION: A first nitride semiconductor layer 5 comprising a p-type impurity is formed on an active layer 4, and on the first nitride semiconductor layer I5, a second nitride semiconductor layer 6 which comprises less p-type impurities than the p-type impurity concentration of the first nitride semiconductor layer 5 is provided. Furthermore, on the second nitride semiconductor layer 6, a third nitride semiconductor layer 7 comprising a more p-type impurity than the p-type impurity concentration of the first nitride semiconductor layer 5 is provided.

[Claim(s)]
[Claim 1] The 1st nitride semiconductor layer which contains p type impurity in the barrier-layer upper part is formed. in the 1st nitride semiconductor layer upper part It has the 2nd nitride semiconductor layer containing p type impurity more nearly little than p type high impurity concentration of the 1st nitride semiconductor layer. The nitride semiconductor device characterized by having the 3rd nitride semiconductor layer which contains a lot of p type impurities than p type high impurity concentration of the 1st nitride semiconductor layer in the 2nd nitride semiconductor layer upper part.
[Claim 2] The nitride semiconductor device according to claim 1 to which p type high impurity concentration of the nitride semiconductor layer of the above 1st is characterized by or more 1x1017 being 1x1020 or less.
[Claim 3] The nitride semiconductor device according to claim 1 or 2 to which p type high impurity concentration of the nitride semiconductor layer of the above 2nd is characterized by being less than 1x1020.
[Claim 4] A nitride semiconductor device given in any 1 term of the claims 1-3 to which p type high impurity concentration of the nitride semiconductor layer of the above 3rd is characterized by or more 1x1018 being 1x1021 or less.
[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the element which consists of a nitride semiconductor (InXAlYGa1-X-YN, 0 <=X, 0<=Y, X+Y<=1) used for photo detectors, such as light emitting devices, such as Light Emitting Diode and LD, a solar battery, and a photosensor, etc.
[0002]
[Description of the Prior Art] The nitride semiconductor was just put in practical use by these people with the full color Light Emitting Diode display, the traffic light, etc. as a material of high brightness blue Light Emitting Diode and authentic green Light Emitting Diode. Light Emitting Diode used for these various devices has terrorism structure to the double by which the barrier layer which consists of InGaN of single quantum well structure (SQW:Single-Quantum-Well) was sandwiched between n type nitride semiconductor layer and p type nitride semiconductor layer. Wavelength,

such as blue and green, is determined by fluctuating In composition ratio of an InGaN barrier layer. Blue Light Emitting Diodes are the luminescence wavelength of 450nm, the half-value width of 20nm, the luminous intensity of 2 cds, 5mW of optical outputs, and 9.1% of external quantum efficiencies in 20mA. On the other hand, similarly green Light Emitting Diodes are the luminescence wavelength of 525nm, the half-value width of 30nm, the luminous intensity of 6 cds, 3mW of optical outputs, and 6.3% of external quantum efficiencies in 20mA.

[0003] Moreover, these people announced the 410nm laser oscillation in a room temperature for the first time under the pulse current in the world recently using this material {Jpn.J.Appl.Phys.35(1996) L74 and Jpn.J.Appl.Phys.35(1996) L217 grade}. This laser element has terrorism structure to the double which has the barrier layer of multiplex quantum well structure which used InGaN, is the conditions of 2 microseconds of pulse width, and 2ms of pulse periods, and shows the oscillation of the threshold current of 610mA, and threshold current density 8.7 kA/cm2,410nm. The improved laser element was also announced in Appl.Phys.Lett.69 (1996) 1477. This laser element has the structure where the ridge stripe was formed in a part of p type nitride semiconductor layer, is 1 microsecond of pulse width, 1ms of pulse periods, and 0.1% of duty ratio, and shows the oscillation of the threshold current of 187mA, and threshold current density 3 kA/cm2,410nm. Furthermore, these people succeeded also in the continuous oscillation in a room temperature for the first time, and announced. A this {Nikkei electronics December 2, 1996 issue technical news flash [for example,], Appl.Phys.Lett.69 (1996) 3034, Appl.Phys.Lett.69 (1996) 4056, etc. and laser} element shows the continuous oscillation of 27 hours in 20 degrees C in threshold current density 3.6 kA/cm2 and a threshold-voltage 5.5V or 1.5mW output.

[0004]

[Problem(s) to be Solved by the Invention] Thus, although the luminescence device using the nitride semiconductor is already put in practical use as a Light Emitting Diode, there is also a still inadequate point and improvement in the further radiant power output is desired. Moreover, LD is under research wholeheartedly now aiming at utilization, and reinforcement is desired not to mention improvement in an output. If the radiant power

output of a luminescence device like these [Light Emitting Diode and LD] can be raised, the light-receiving efficiency of light-receiving devices, such as a solar battery and a photosensor, in which it has similar structure can also be raised simultaneously. Therefore, the place which accomplishes this invention in view of such a situation, and is made into the purpose is by offering the nitride semiconductor device which has new structure to mainly raise the output of Light Emitting Diode and LD.

[0005]

[Means for Solving the Problem] That is, the following composition can attain this invention.

(1) The 1st nitride semiconductor layer which contains p type impurity in the barrier-layer upper part is formed. It has the 2nd nitride semiconductor layer which contains p type impurity more nearly little than p type high impurity concentration of the 1st nitride semiconductor layer in the 1st nitride semiconductor layer upper part. The nitride semiconductor device characterized by having the 3rd nitride semiconductor layer which contains a lot of p type impurities than p type high impurity concentration of the 1st nitride semiconductor layer in the 2nd nitride semiconductor layer upper part.

(2) A nitride semiconductor device given in the above (1) whose p type high impurity concentration of the nitride semiconductor layer of the above 1st is characterized by or more 1x1017 being 1x1020 or less.

(3) The above (1) whose p type high impurity concentration of the nitride semiconductor layer of the above 2nd is characterized by being less than 1x1020, or a nitride semiconductor device given in (2).

(4) A nitride semiconductor device given in any 1 term of aforementioned (1) - (3) to which p type high impurity concentration of the nitride semiconductor layer of the above 3rd is characterized by or more 1x1018 being 1x1021 or less.

[0006] That is, the output of Light Emitting Diode and LD can be raised by specifying the order of a laminating of two or more p side nitride semiconductor layers in which this invention specified p type high impurity concentration of two or more p side nitride semiconductor layers of the specification by which a laminating is carried out to the upper part of a barrier layer, and p type high impurity concentration was specified further.

In addition, in this invention, a barrier layer and the 1st nitride semiconductor layer touch, and it does not need to be formed, and the 1st nitride semiconductor layer and the 2nd nitride semiconductor layer touch, and it does not need to be formed, and further, the 2nd nitride semiconductor layer and the 3rd nitride semiconductor layer touch, and do not need to be formed.

[0007]

[Embodiments of the Invention] Drawing 1 is the typical cross section showing the structure of the nitride semiconductor device which is the gestalt of 1 operation of this invention, and specifically shows the structure of a Light Emitting Diode element. The buffer layer 2 which consists of GaN as element structure on the substrate 1 which consists of sapphire, the n side contact layer 3 (** n side clad layer) which consists of an Si dope GaN, The barrier layer 4 which consists of InGaN of the single quantum well structure of 30A of thickness, the 1st p side nitride semiconductor layer 5 which consists of a Mg dope AlGaN, the 2nd p side nitride semiconductor layer 6 which Mg becomes from GaN by which the little dope was carried out rather than the 1st p side nitride semiconductor layer 5, It has come to carry out the laminating of the 3rd p side nitride semiconductor layer 7 which Mg becomes from doped GaN. Mostly, the p electrode 8 of the 3rd p side nitride semiconductor layer 7 which becomes the whole surface from the metal thin film of a translucency is formed, and the pad electrode 9 for bondings is formed in the corner of the whole surface electrode 8. The n electrode 10 is formed in the front face of the n side contact layer 3 **********ed and exposed from the p side nitride semiconductor layer side on the other hand.

[0008] Like the above, the element of this invention can raise a light-emitting-device output by forming the 3rd p side nitride semiconductor layer to which many 2nd p side nitride semiconductor layer specify the p side high impurity concentration few, and much p side high impurity concentration were specified in order of a specific laminating to the concentration of the p side impurity of the 1st p side nitride semiconductor layer. Namely, the 3rd p side nitride semiconductor layer by which p type impurity which acts as a contact layer was doped by high concentration, The 2nd p side nitride semiconductor layer by which p type impurity was doped by the position which approached the barrier layer rather than the 3rd p side nitride

semiconductor layer fewer than the 1st p side nitride semiconductor layer, The output of the whole element can be raised by having the 1st p side nitride semiconductor layer by which more [it is fewer than the 3rd, and] p type impurities than the 2nd were doped by the position which furthermore approached the barrier layer rather than the 2nd nitride semiconductor.

[0009] A barrier layer 4 is taken as the single quantum well structure containing the nitride semiconductor layer which contains In at least, or multiplex quantum well structure. As for a well layer, it is [100A or less of thickness] still more preferably desirable to constitute from InXGa1-XN (0< X<=1) 70A or less, and, as for a barrier layer, it is desirable to constitute still more preferably 200A or less of InYAlZGa1-Y-ZN with larger bandgap energy than a well layer (0<=Y, 0<=Z, Y+Z<=1) from thickness 150A or less.

[0010] That what is necessary is just to consist of nitride semiconductor layers containing p type impurity, even if the 1st p side nitride semiconductor layer 5 is in contact with especially the barrier layer, it does not need to be. The large nitride semiconductor of bandgap energy is chosen from a barrier layer as a semiconductor, for example, AlXGa1-XN (0<=X<=1) is grown up preferably as mentioned above. p type high impurity concentration doped in the 1st p side nitride semiconductor layer 5 is more preferably adjusted to 1x1019-/cm3 three or more 1x1018-/cm three or more 1x1017-/cm and three or less 1x1020-/cm. However, it is adjusted so that it may become less than the 3rd nitride semiconductor layer more mostly within the limits of this than the 2nd nitride semiconductor layer. It is a book that p type high impurity concentration is the above-mentioned range. As a p type impurity which can be doped in 1st p type nitride semiconductor layer 5, II group elements, such as Mg, Zn, Cd, calcium, Be, and Sr, are doped preferably, for example. Furthermore, two kinds of nitride semiconductor layers from which composition differs mutually can also use this 1st nitride semiconductor layer as the superlattice layer which comes to carry out a laminating. When considering as a superlattice layer, 100A or less of 70A or less of thickness of the nitride semiconductor layer which constitutes a superlattice layer is most preferably adjusted to thickness 50A or less still more preferably. It is desirable in respect of a radiant power output and forward voltage in thickness being this range. Moreover, in this invention, if the 1st nitride semiconductor layer 5 is used as a superlattice layer, the

crystallinity of a nitride semiconductor layer will become good and an output will improve further. When considering as a superlattice layer, p type impurity may be doped in both layers, and may be doped in one of layers.

[0011] Although it is desirable to be formed in contact with the 1st nitride semiconductor layer 5 as for the 2nd nitride semiconductor layer 6, it does not need to be touched and formed especially. For example, the nitride semiconductor layer of undoping of thickness hundreds of A or less can also be grown up between the 1st and the 2nd nitride semiconductor layer. adjusting p type impurity doped by the 2nd nitride semiconductor layer 6 so that it may become less than each the 1st and 3rd nitride semiconductor layers 5 and 6 -- desirable -- concrete -- less than three 1x1020-/cm -- desirable -- 1x1019-/cm -- it adjusts to 1x1018-/cm3 more preferably the 3 bottom Moreover, as for the 2nd nitride semiconductor layer, the impurity does not need to be doped. Moreover, it is adjusted so that it may become less than each the 1st and 3rd nitride semiconductor layers within the limits of this. It is a book that p type high impurity concentration is the above-mentioned range. What has p type impurity [be / the same as that of the impurity which can be doped in the 1st nitride semiconductor layer / it] doped by the 2nd nitride semiconductor layer is mentioned. Although especially composition of the 2nd nitride semiconductor layer is not asked, it is preferably considered as the same composition as the 3rd nitride semiconductor layer. 2 micrometers or less of 1 micrometer or less of thickness of the 2nd nitride semiconductor layer are most preferably adjusted to 0.5 micrometers or less still more preferably. It is desirable in respect of a radiant power output and forward voltage in thickness being this range. Moreover, you may make p type high impurity concentration of the nitride semiconductor layer which constitutes the multilayer for the 2nd nitride semiconductor layer as multilayer (superlattice is included) structure of a nitride semiconductor decrease gradually.

[0012] If it is desirable to consider as the contact layer which forms p electrode as for the 3rd nitride semiconductor layer 7 and X value sets to 0.3 or less AlXGa1-XN (0<=X<=0.3) preferably, p electrode and desirable OMIKKU will be obtained. As for p type high impurity concentration of the 3rd nitride semiconductor layer 7, it is preferably desirable more preferably to adjust to 2x1020-/cm3 three or more 1x1019-/cm three or more 1x1018-/cm

and three or less 1x1021-/cm. Moreover, it is adjusted so that it may increase more than each the 1st and 2nd nitride semiconductor layers within the limits of this. It is a book that p type high impurity concentration is the above-mentioned range. Moreover, as for the thickness of the 3rd nitride semiconductor layer, it is desirable to adjust more thinly than the 2nd nitride semiconductor layer. That is, thickness of 3rd p type nitride semiconductor layer which acts as a contact layer is made thin, and since contact resistance falls by doping p type impurity to high concentration, it is in the inclination for Vf (forward voltage) to tend to fall. 1 micrometer or less 0.1 micrometers or less is specifically as thickness of the 3rd nitride semiconductor layer most preferably adjusted to 0.05 micrometers or less still more preferably. It is desirable in respect of a radiant power output and forward voltage in thickness being this range.

[0013] Moreover, especially the composition of constituting the nitride semiconductor device of this invention and others should just be an object which is not limited but fills the composition of the above-mentioned this invention at least.

[0014]

[Example] Hereafter, although the example of this invention is shown, this invention is not limited to this. In the example of this invention, a nitride semiconductor device is manufactured using the MOCVD method.

[0015] The substrate which makes a [example 1] sapphire (0001) side a principal plane is prepared, and the buffer layer which uses TMG (trimethylgallium) and ammonia for material gas, and consists of GaN at 500 degrees C is grown up by 200A thickness.

[0016] Next, temperature is raised at 1050 degrees C, mono-silane gas is used for TMG, ammonia, and impurity gas, and the n type GaN layer which doped Si 1x1019-/cm3 is grown up by 5-micrometer thickness.

[0017] Next, temperature is made into 800 degrees C and the well layer which consists of undoping In0.4Ga0.6N is grown up by 25A thickness as a barrier layer using TMI (trimethylindium), TMG, and ammonia.

[0018] Next, temperature is made into 1050 degrees C and the 1st nitride semiconductor layer which consists of p type aluminum0.3Ga0.7N which doped Mg 1x1019-/cm3 is grown up by 200A thickness, using Cp2Mg (magnesium cyclopentadienyl) as TMG, ammonia, and impurity gas. This 1st

nitride semiconductor layer acts as a layer which shuts up a carrier.

[0019] Material gas is stopped after the 1st nitride semiconductor layer growth, TMG, ammonia, and Cp2Mg are poured again continuously, and the 2nd nitride semiconductor layer which consists of GaN which doped Mg 1x1018-/cm3 at 1050 degrees C is grown up by 0.18-micrometer thickness.

[0020] The 3rd nitride semiconductor layer which doped Mg 2x1020-/cm3 is grown up by 300A thickness after the 2nd nitride semiconductor layer growth using TMG, ammonia, and Cp2Mg.

[0021] Annealing is performed for the wafer into which the nitride semiconductor was grown up as mentioned above at 700 degrees C among nitrogen atmosphere in a reaction container, and the layer which doped p type impurity is made to form into low resistance further. A wafer is picked out from a reaction container after annealing, an RIE system performs etching from a 3rd [of the best layer] nitride semiconductor layer side, and the front face of the n side contact layer which should form n electrode is exposed. Mostly, the whole surface electrode of the 3rd nitride semiconductor layer of the best layer which becomes the whole surface from nickel/Au is formed by 200A thickness, and the pad electrode which turns into a part of the whole surface electrode from Au by 1-micrometer thickness is formed. On the other hand, n electrode which consists of W and Au is formed in the front face of the exposed n side contact layer.

[0022] When it separated into the chip of 350-micrometer angle and the wafer which formed the electrode as mentioned above was made to emit light, in 20mA, it became Vf3.2V, the luminescence wavelength of 525nm, 3.5mW of optical outputs, and 7.3% of external quantum efficiencies, and improved by about 1.3 times as compared with the conventional green Light Emitting Diode.

[0023] In the [example 2] example 1, Mg was doped 5x1019-/cm3 in the 1st nitride semiconductor layer, Mg was doped 5x1017-/cm3 in the 2nd nitride semiconductor layer, Mg was doped 1x1020-/cm3 in the 3rd nitride semiconductor layer, and when others were performed similarly, they were able to obtain the Light Emitting Diode element which has the almost same property as an example 1.

[0024] [Example 3] drawing 2 is the typical cross section showing the structure of the 1 laser element concerning this invention, and explains the

3rd example of this invention hereafter based on this drawing.

[0025] The GaN substrate 100 into which the single crystal which consists of GaN through the buffer layer which consists of GaN on the substrate which makes a sapphire (0001) side a principal plane was grown up by 120-micrometer thickness is prepared. In the state where it was made to grow up on sapphire, this GaN substrate 100 is set in a reaction container, temperature is raised to 1050 degrees C, and the n side buffer layer 11 which consists of GaN which doped Si 1x1018-/cm3 on the GaN substrate 100 like an example 1 is grown up by 4-micrometer thickness. This n side buffer layer is a buffer layer grown up at an elevated temperature, for example, the buffer layer 2 which grows up GaN, AlN, etc. directly by thickness 0.5 micrometers or less in low temperature 900 degrees C or less on the substrate which consists of sapphire, SiC, and a different material from a nitride semiconductor like a spinel like an example 1 is distinguished.

[0026] (n side clad layer 12= strained super lattice layer) then, the 1st layer which consists of n type aluminum0.3Ga0.7N which doped Si 1x1019-/cm3 using TMA (trimethylaluminum), TMG, ammonia, and silane gas at 1050 degrees C -- 40 O It is made to grow up by the thickness of NGUSUTO loam, and silane gas and TMA are stopped continuously and the 2nd layer which consists of GaN of undoping is grown up by 40A thickness. and 1st layer + 2nd layer + 1st layer + 2nd layer + ... as -- a strained super lattice layer is constituted, the laminating of every 100 layers is carried out by turns, respectively, and the n side clad layer 12 which consists of a strained super lattice of the 0.8 micrometers of the total thickness is grown up

[0027] (n photometry guide layer 13) Then, silane gas is stopped and n photometry guide layer 13 which consists of undoping GaN at 1050 degrees C is grown up by 0.1-micrometer thickness. As for this n photometry guide layer, it is desirable to act as a light-guide layer of a barrier layer, and to grow up GaN and InGaN, and it is usually desirable to make it grow up by 200A - 1 micrometer thickness still more preferably 100A - 5 micrometers. Moreover, it can also consider as the strained super lattice layer of undoping of this layer. In considering as a strained super lattice layer, bandgap energy is larger than a barrier layer, and it makes it smaller than the n side clad layer.

[0028] (Barrier layer 14) Next, TMG, TMI, and ammonia are used for

material gas, and a barrier layer 14 is grown up. A barrier layer 14 holds temperature at 800 degrees C, and grows up the well layer which consists of undoping In0.2Ga0.8N by 25A thickness. Next, the barrier layer which consists of undoping In0.01Ga0.95N at the same temperature only by changing the mole ratio of TMI is grown up by 50A thickness. This operation is repeated twice and the barrier layer of the multiplex quantum well structure (MQW) of the 175A of the total thickness which carried out the laminating of the well layer to the last is grown up. Undoping is sufficient as a barrier layer like this example, and it may dope n type impurity and/or p type impurity. An impurity may be doped to both a well layer and a barrier layer, and may be doped to either.

[0029] (p side cap layer 15) Next, temperature is raised to 1050 degrees C and the p side cap layer 17 which consists of p type aluminum0.3Ga0.7N with larger bandgap energy which doped Mg 1x1019-/cm3 than p photometry guide layer 16 is grown up by 300A thickness using TMG, TMA, ammonia, and Cp2Mg (magnesium cyclopentadienyl). If the p side cap layer is grown up by thickness 0.1 micrometers or less, since it will act still more preferably 0.5 micrometers or less as a barrier for the p side cap layer shutting up a carrier in a barrier layer, its output improves. Although especially the minimum of the thickness of this p type cap layer 15 does not limit, it is desirable to form by thickness 10A or more.

[0030] (p photometry guide layer 16) p photometry guide layer 16 which consists of GaN to which Mg with bandgap energy smaller than the p side cap layer 15 was doped 1x1020-/cm3 at 1050 degrees C like the example 1 using TMG, Cp2Mg, and ammonia again after p side cap layer 15 growth is grown up by 0.1-micrometer thickness. This layer acts as a light-guide layer of a barrier layer.

[0031] (p side clad layer 17= 1st nitride semiconductor layer) Then, the layer which consists of p type aluminum0.3Ga0.8N which doped Mg 1x1020-/cm3 at 1050 degrees C is grown up by 40A thickness, only TMA is stopped continuously and the layer which consists of p type GaN which doped Mg 1x1019-/cm3 is grown up by 40A thickness. And this operation is repeated 100 times, respectively and the p side clad layer 17 which consists of a strained super lattice layer of the 0.8 micrometers of the total thickness is formed. The average concentration of Mg of the p side clad layer is 5x1019-

/cm3.

[0032] At the end, (p side contact layer 18= the 2nd and the 3rd nitride semiconductor layer) At 1050 degrees C The layer (2nd nitride semiconductor layer) which consists of p type GaN which doped Mg 1x1018-/cm3 on the p side clad layer 17 is grown up by 0.1-micrometer thickness. Then, the layer (3rd nitride semiconductor layer) which consists of p type GaN which doped Mg 2x1020-/cm3 is grown up by 200A thickness. The p side contact layer 18 can be constituted from p type InXAlYGa1-X-YN (0 <=X, 0<=Y, X+Y<=1), and GaN which doped Mg preferably, then the p electrode 21 and the most desirable ohmic contact are obtained. Moreover, since the p side clad layer 17 of the strained super lattice structure containing p mold AlYGa1-YN is touched and the thickness is made thin with 500A or less by using the small nitride semiconductor of bandgap energy as the p side contact layer, the carrier concentration of the p side contact layer 18 becomes high substantially, p electrode and desirable OMIKKU are obtained, and the threshold current of an element and voltage fall.

[0033] Annealing is performed for the wafer into which the nitride semiconductor was grown up as mentioned above at 700 degrees C among nitrogen atmosphere in a reaction container, and the layer which doped p type impurity is made to form into low resistance further.

[0034] As a wafer is picked out from a reaction container after annealing and it is shown in drawing 3, the p side contact layer 18 of the best layer and the p side clad layer 17 are **********ed by the RIE system, and it considers as the ridge configuration which has stripe width of face of 4 micrometers. Thus, by making into a stripe-like ridge configuration the layer which exists above a barrier layer, luminescence of a barrier layer comes to concentrate on the bottom of a stripe ridge, and a threshold falls. It is desirable to make into a ridge configuration a 17 or more p side clad layers [which consist especially of strained super lattice layers] layer.

[0035] The p electrode 21 which consists of nickel/Au is formed in the ridge maximum front face of the p side contact layer 18 in the shape of a stripe after ridge formation, the insulator layer 25 which becomes a nitride semiconductor layer's on the front faces of the maximum other than p electrode 21 from SiO2 is formed, and p pad electrode 22 which connected with the p electrode 21 electrically through this insulator layer 25 is formed.

[0036] The wafer which formed p electrode as mentioned above is transported to polish equipment, polish removes silicon on sapphire, and the front face of the GaN substrate 10 is exposed. The n electrode 23 of the exposed GaN substrate front face which becomes the whole surface from Ti/aluminum is formed mostly.

[0037] A cleavage is carried out by the Mth page (field which is equivalent to the side of a hexagonal prism when a nitride semiconductor is approximated by hexagonal system) of the GaN substrate after electrode formation, and the dielectric multilayer which becomes the cleavage plane from SiO2 and TiO2 is formed, and finally, in a direction parallel to p electrode, a bar is cut and it considers as a laser element.

[0038] When this laser chip was installed in the heat sink by the face up (state which the substrate and the heat sink countered), wire bonding of each electrode was carried out and laser oscillation was tried at the room temperature, in the room temperature, by threshold current density 2.0 kA/cm2 and threshold-voltage 4.0V, continuous oscillation with an oscillation wavelength of 405nm was checked, and the life of 1000 hours or more was shown.

[0039]

[Effect of the Invention] Thus, in the nitride semiconductor device of this invention, an output can be sharply raised by specifying the concentration of p type impurity of two or more nitride semiconductor layers by which a laminating is carried out on a barrier layer in the specific range, and specifying the order of a laminating. Moreover, the element of this invention can be used for many electron devices using a nitride semiconductor not only like Light Emitting Diode and a luminescence device like LD but other light-receiving devices.

[Brief Description of the Drawings]

[Drawing 1] It is the type section view showing the structure of the Light Emitting Diode element concerning one example of this invention.

[Drawing 2] It is the type section view showing the structure of LD element concerning other examples of this invention.

[Description of Notations]

1 ... Substrate

2 ... Buffer layer

3 ... The n side contact layer
4 ... Barrier layer
5 ... The 1st p side nitride semiconductor layer
6 ... The 2nd p side nitride semiconductor layer
7 ... The 3rd p side nitride semiconductor layer
8 ... p electrode
9 ... Pad electrode
10 ... n electrode

Fig. 1

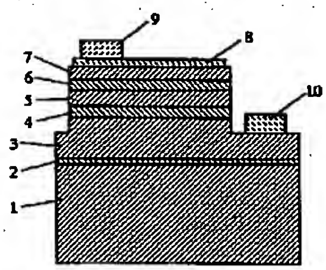

9
8
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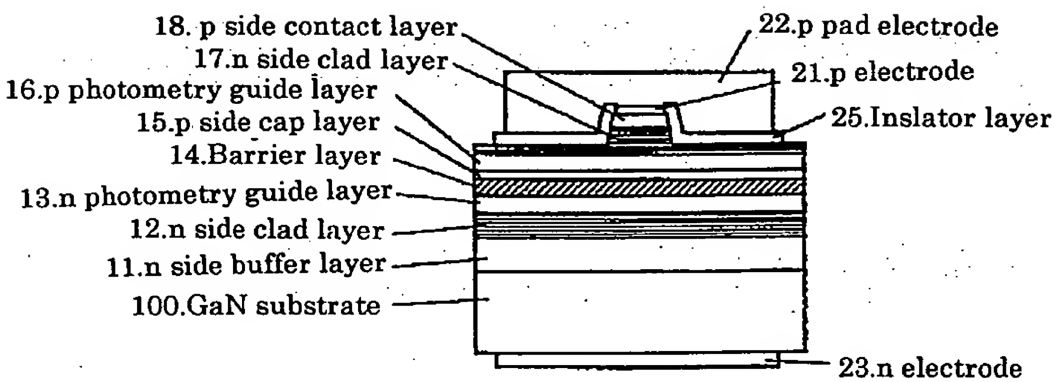
Fig. 2


18. p side contact layer
17.n side clad layer
16.p photometry guide layer
15.p side cap layer
14.Barrier layer
13.n photometry guide layer
12.n side clad layer
11.n side buffer layer
100.GaN substrate
22.p pad electrode
21.p electrode
25.Inslator layer
23.n electrode

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LD w/
m-plane cleavage [0037]

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(57)【要約】

(57)[SUMMARY]

【目的】
新規な窒化物半導体素子の構造を提供することにより、ＬＥＤ、ＬＤの出力を向上させる。

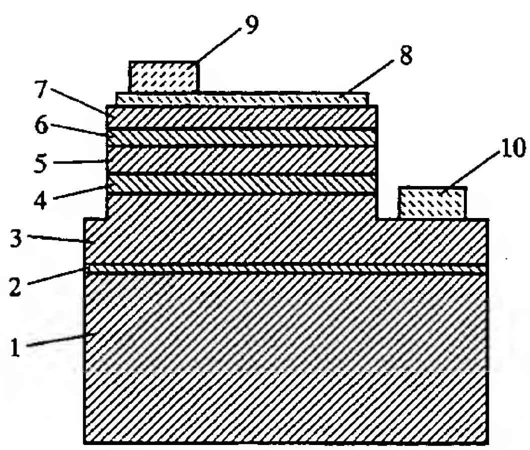
[OBJECT]
The output of LED and LD is improved by providing the structure of a novel nitride semiconductor element.

【構成】
活性層４上部にｐ型不純物を含む第１の窒化物半導体層５が形成され、その第１の窒化物半導体層５上部に、その第１の窒化物半導体層５のｐ型不純物濃度より少量のｐ型不純物を含む第２の窒化物半導体層６を備え、その第２の窒化物半導体層６上部に、第１の窒化物半導体層５のｐ型不純物濃度よりも多量のｐ型不純物を含む第３の窒化物半導体層７を有する。

[SUMMARY OF THE INVENTION]
The first nitride semiconductor layer 5 which includes a p-type impurity in the active-layer 4 upper part is formed.

The 2nd nitride semiconductor layer 6 which includes a smaller amount of p-type impurity than the p-type impurity concentration of that first nitride semiconductor layer 5 is provided in that first nitride semiconductor layer 5 upper part.

It has the third nitride semiconductor layer 7 which includes a lot of p-type impurities than the p-type impurity concentration of the first nitride semiconductor layer 5 in that 2nd nitride semiconductor layer 6 upper part.



【特許請求の範囲】

[CLAIMS]

【請求項１】
活性層上部にｐ型不純物を含む

[CLAIM 1]
The first nitride semiconductor layer which

第１の窒化物半導体層が形成され、その第１の窒化物半導体層上部に、その第１の窒化物半導体層のｐ型不純物濃度より少量のｐ型不純物を含む第２の窒化物半導体層を備え、その第２の窒化物半導体層上部に、第１の窒化物半導体層のｐ型不純物濃度よりも多量のｐ型不純物を含む第３の窒化物半導体層を有することを特徴とする窒化物半導体素子。

includes a p-type impurity in the active-layer upper part is formed. The 2nd nitride semiconductor layer which includes smaller amount of p-type impurity than the p-type impurity concentration of that first nitride semiconductor layer is provided in that first nitride semiconductor layer upper part.

It has the third nitride semiconductor layer which includes a lot of p-type impurities than the p-type impurity concentration of a first nitride semiconductor layer in that 2nd nitride semiconductor layer upper part.

A nitride semiconductor element characterized by the above-mentioned.

【請求項２】

前記第１の窒化物半導体層のｐ型不純物濃度が、$１×１０^{17}$以上$１×１０^{20}$以下であることを特徴とする請求項１に記載の窒化物半導体素子。

[CLAIM 2]

The p-type impurity concentration of a first nitride semiconductor layer is 1*1017 or more 1*1020 or less.

A nitride semiconductor element described in Claim 1 characterized by the above-mentioned.

【請求項３】

前記第２の窒化物半導体層のｐ型不純物濃度が、$１×１０^{20}$未満であることを特徴とする請求項１又は２に記載の窒化物半導体素子。

[CLAIM 3]

The p-type impurity concentration of a second nitride semiconductor layer is less than 1*1020.

A nitride semiconductor element of Claims 1 and 2 characterized by the above-mentioned.

【請求項４】

前記第３の窒化物半導体層のｐ型不純物濃度が、$１×１０^{18}$以上$１×１０^{21}$以下であることを特徴とする請求項１～３のいずれか１項に記載の窒化物半導体素子。

[CLAIM 4]

The p-type impurity concentration of a third nitride semiconductor layer is 1*1018 or more 1*1021 or less.

A nitride semiconductor element described in any 1 item of Claim 1 - 3 characterized by the above-mentioned.

【発明の詳細な説明】

[DETAILED DESCRIPTION OF INVENTION]

【０００１】

[0001]

【産業上の利用分野】

[INDUSTRIAL APPLICATION]

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本発明は例えばＬＥＤ、ＬＤ等の発光素子、太陽電池、光センサー等の受光素子等に用いられる窒化物半導体（Ｉｎ$_X$Ａｌ$_Y$Ｇａ$_{1-X-Y}$Ｎ、０≦Ｘ、０≦Ｙ、Ｘ＋Ｙ≦１）よりなる素子に関する。

This invention relates to the element which consists of the nitrid semiconductor (InXAlYGa1-X- YN, 0=<X, 0=<Y, X+Y=<1) used, for example, for a LED and LD etc. light-emitting element, light receiving elements, such as a solar battery and a photo sensor, etc.

【０００２】

[0002]

【従来の技術】

窒化物半導体は高輝度青色ＬＥＤ、純緑色ＬＥＤの材料として、本出願人により、フルカラーＬＥＤディスプレイ、交通信号等で実用化されたばかりである。これらの各種デバイスに使用されるＬＥＤは、ｎ型窒化物半導体層とｐ型窒化物半導体層との間に、単一量子井戸構造（ＳＱＷ：Single-Quantum- Well）のＩｎＧａＮよりなる活性層が挟まれたダブルヘテロ構造を有している。青色、緑色等の波長はＩｎＧａＮ活性層のＩｎ組成比を増減することで決定されている。青色ＬＥＤは２０ｍＡにおいて発光波長４５０ｎｍ、半値幅２０ｎｍ、光度２ｃｄ、光出力５ｍW、外部量子効率９．１％である。一方、緑色ＬＥＤは同じく２０ｍＡにおいて、発光波長５２５ｎｍ、半値幅３０ｎｍ、光度６ｃｄ、光出力３ｍW、外部量子効率６．３％である。

[PRIOR ART]

The nitride semiconductor was just utilized by this applicant by the full-color LED display, the traffic signal, etc. as material of the high-intensity blue LED and the pure green LED.

LED used to these various devices has the double heterostructure by which the active layer which consists of InGaN of the single quantum well structure (SQW:Single-Quantum-Well) was pinched between,n-type nitride semiconductor layer and the p-type nitride semiconductor layer.

Wavelengths, such as blue and green, are determined by fluctuating In composition ratio of InGaN active layer.

Blue LED is the light-emission wavelength of 450 nm, the half value width of 20 nm, the luminous intensity of 2 cd, 5 mW of optical powers, and 9.1% of external quantum efficiencies in 20mA.

On the other hand, green LED is the light-emission wavelength of 525 nm, the half value width of 30 nm, the luminous intensity of 6 cd, 3 mW of optical powers, and 6.3% of external quantum efficiencies in 20mA similarly.

【０００３】

また本出願人は、最近この材料を用いてパルス電流下、室温での４１０ｎｍのレーザ発振を世界で初めて発表した{例えば、Jpn.J.Appl.Phys.35(1996)L74 、

[0003]

Moreover this applicant announced recently the 410 nm laser oscillation in a room temperature under the pulse current for the first time in the world using this material. {For example, such as Jpn.J.Appl.Phys.35(1996) L74, and Jpn.J.Appl.Phys.35(1996) L217}, this laser

Jpn.J.Appl.Phys.35(1996)L217等}。このレーザ素子は、ＩｎＧａＮを用いた多重量子井戸構造の活性層を有するダブルヘテロ構造を有し、パルス幅２μｓ、パルス周期２ｍｓの条件で、閾値電流６１０ｍＡ、閾値電流密度８．７ｋＡ／cm²、４１０ｎｍの発振を示す。改良したレーザ素子もまた、Appl.Phys.Lett.69(1996)1477において発表した。このレーザ素子は、ｐ型窒化物半導体層の一部にリッジストライプが形成された構造を有しており、パルス幅１μｓ、パルス周期１ｍｓ、デューティー比０．１％で、閾値電流１８７ｍＡ、閾値電流密度３ｋＡ／cm²、４１０ｎｍの発振を示す。さらに本出願人は室温での連続発振にも初めて成功し、発表した。{例えば、日経エレクトロニクス 1996 年 12 月 2 日号 技術速報、Appl.Phys.Lett.69(1996)3034、Appl.Phys.Lett.69(1996)4056等}、このレーザ素子は２０℃において、閾値電流密度３．６ｋＡ／cm²、閾値電圧５．５Ｖ、１．５ｍW出力において、２７時間の連続発振を示す。

element has the double heterostructure which has the active layer of the multiquantum well structure using InGaN.

The conditions of a 2 μs pulse width and 2ms of pulse periods show 610mA of threshold-value currents, 8.7kA/a cm-squared threshold-value current density, and a 410 nm oscillation.

The improved laser element was also announced in Appl.Phys.Lett.69 (1996) 1477.

This laser element has the structure where the ridge stripe was formed in a part of p-type nitride semiconductor layer.

1 μs pulse width, 1ms of pulse periods, and 0.1% of duty ratios show 187mA of threshold-value currents, 3kA/a cm-squared threshold-value current density, and a 410 nm oscillation. Furthermore this applicant succeed also in the continuous oscillation in a room temperature for the first time and announced.

{For example, Nikkei electronics December 2nd 1996 issue, technical news flash, Appl.Phys.Lett.69 (1996) 3034, and Appl.Phys.Lett.69 (1996) 4056,}, This laser element shows the continuous oscillation of 27 hours in 3.6kA/cm-squared threshold-value current density, threshold-voltage 5.5V, and 1.5 mW output in 20 degree C.

【０００４】

[0004]

【発明が解決しようとする課題】

このように窒化物半導体を用いた発光デバイスはＬＥＤとして既に実用化されているが、未だ不十分な点もあり、さらなる発光出力の向上が望まれている。

[PROBLEM ADDRESSED]

The light-emission device using the nitride semiconductor in this way sets to LED, and is already utilized.

However, there is also a still inadequate point.

The improvement in the further light-emission output is desired.

またＬＤは実用化を目指して現在鋭意研究中であり、出力の向上はもちろんのこと、長寿命化が望まれている。これらＬＥＤ、ＬＤのような発光デバイスの発光出力を向上させることができれば、類似した構造を有する太陽電池、光センサー等の受光デバイスの受光効率も同時に向上させることができる。従って、本発明はこのような事情を鑑みて成されたものであって、その目的とするところは、新規な構造を有する窒化物半導体素子を提供することにより、主としてＬＥＤ、ＬＤの出力を向上させることにある。

Moreover LD is under research zealously currently aiming at utilization.

The long life is desired not to mention the improvement in output.

If the light-emission output of these light-emission device such as LED and LD can be improved, the light-receiving efficiency of light-receiving devices, such as the solar battery and a photo sensor, which has the similar structure, can also be improved simultaneously.

Therefore, this invention is formed in view of such a situation.

That objective is to mainly improve the output of LED and LD by providing the nitride semiconductor element which has a novel structure.

【０００５】

[0005]

【課題を解決するための手段】即ち、本発明は以下の構成によって達成することができる。

（１）　活性層上部にｐ型不純物を含む第１の窒化物半導体層が形成され、その第１の窒化物半導体層上部に、その第１の窒化物半導体層のｐ型不純物濃度より少量のｐ型不純物を含む第２の窒化物半導体層を備え、その第２の窒化物半導体層上部に、第１の窒化物半導体層のｐ型不純物濃度よりも多量のｐ型不純物を含む第３の窒化物半導体層を有することを特徴とする窒化物半導体素子。

（２）　前記第１の窒化物半導体層のｐ型不純物濃度が、１×１０^{17}以上１×１０^{20}以下であることを特徴とする前記（１）に記載の窒化物半導体素子。

[SOLUTION OF THE INVENTION]

That is, the following components can attain this invention.

(1) The first nitride semiconductor layer which includes a p-type impurity in the active-layer upper part is formed.

The 2nd nitride semiconductor layer which includes smaller amount of p-type impurity than the p-type impurity concentration of that first nitride semiconductor layer is provided in that first nitride semiconductor layer upper part.

It has the third nitride semiconductor layer which includes a lot of p-type impurities than the p-type impurity concentration of a first nitride semiconductor layer in that 2nd nitride semiconductor layer upper part.

A nitride semiconductor element characterized by the above-mentioned.

(2) The p-type impurity concentration of a first nitride semiconductor layer is 1*1017 or more 1*1020 or less.

A nitride semiconductor element described in an above mentioning (1) characterized by the above-mentioned.

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（３） 前記第２の窒化物半導体層のｐ型不純物濃度が、1×10^{20}未満であることを特徴とする前記（１）又は（２）に記載の窒化物半導体素子。

（４） 前記第３の窒化物半導体層のｐ型不純物濃度が、1×10^{18}以上1×10^{21}以下であることを特徴とする前記（１）～（３）のいずれか１項に記載の窒化物半導体素子。

(3) The p-type impurity concentration of a second nitride semiconductor layer is less than 1*1020.

A nitride semiconductor element described in above-mentioned (1) or (2) characterized by the above-mentioned.

(4) The p-type impurity concentration of an above-mentioned third nitride semiconductor layer is 1*1018 or more 1*1021 or less.

A nitride semiconductor element described in any 1 item of above-mentioning (1)-(3) characterized by the above-mentioned.

【０００６】

つまり、本発明は活性層の上部に積層される特定の複数のｐ側窒化物半導体層のｐ型不純物濃度を規定し、更にｐ型不純物濃度を規定された複数のｐ側窒化物半導体層の積層順を規定することで、ＬＥＤ、ＬＤの出力を向上させることができるものである。なお本発明において、活性層と第１の窒化物半導体層とは接して形成されていなくても良く、また第１の窒化物半導体層と、第２の窒化物半導体層とは接して形成されていなくても良く、さらに第２の窒化物半導体層と第３の窒化物半導体層とは接して形成されていなくても良い。

[0006]

In other words, this invention stipulates the p-type impurity concentration of several specific p side nitride semiconductor layer laminated by the upper part of an active layer.

Furthermore the output of LED and LD can be improved by stipulating the order of a lamination of several p side nitride semiconductor layer in which the p-type impurity concentration was stipulated.

In addition in this invention, an active layer and a first nitride semiconductor layer do not need to be formed in contact. Moreover a first nitride semiconductor layer and a 2nd nitride semiconductor layer do not need to be formed in contact. Furthermore a 2nd nitride semiconductor layer and a third nitride semiconductor layer do not need to be formed in contact.

【０００７】

[0007]

【発明の実施の形態】

図１は本発明の一実施の形態である窒化物半導体素子の構造を示す模式的な断面図であり、具体的にはＬＥＤ素子の構造を示している。素子構造としては、サファイアよりなる基板１の上

[Embodiment]

Fig. 1 is a model sectional view showing the structure of the nitride semiconductor element which is the one embodiment of this invention.

The structure of LED element is shown specifically.

As the element structure, On the substrate 1 which consists of sapphire, the buffer layer 2

に、ＧａＮよりなるバッファ層２、ＳｉドープＧａＮよりなるｎ側コンタクト層３（兼ｎ側クラッド層）、膜厚３０オングストロームの単一量子井戸構造のＩｎＧａＮよりなる活性層４、ＭｇドープＡｌＧａＮよりなる第１のｐ側窒化物半導体層５、Ｍｇが第１のｐ側窒化物半導体層５よりも少量ドープされたＧａＮよりなる第２のｐ側窒化物半導体層６、Ｍｇが第１のｐ側窒化物半導体層５よりも多くドープされたＧａＮよりなる第３のｐ側窒化物半導体層７が積層されてなっている。第３のｐ側窒化物半導体層７のほぼ全面には、透光性の金属薄膜よりなるｐ電極８が形成され、その全面電極８の隅部にはボンディング用のパッド電極９が形成されている。一方ｐ側窒化物半導体層側からエッチングして露出されたｎ側コンタクト層３の表面にはｎ電極１０が形成されている。

which consists of GaN, n side contact layer 3 which consists of Si dope GaN (and n side clad layer), the active layer 4 which consists of InGaN of the single quantum well structure of 30 angstroms film thickness, the first p side nitride semiconductor layer 5 which consists of Mg dope AlGaN, the 2nd p side nitride semiconductor layer 6 which consists of GaN by which smaller-amount dope of the Mg was performed than the first p side nitride semiconductor layer 5, the third p side nitride semiconductor layer 7 which consists of GaN by which more Mg than the first p side nitride semiconductor layer 5 was doped It has been to laminate an above.

To almost whole surface of the third p side nitride semiconductor layer 7, the p electrode 8 which consists of the metal thin film of a permeability is formed. The pad electrode 9 for bonding is formed in the corner of that whole-surface electrode 8.

On the other hand, the n electrode 10 is formed in the surface of n side contact layer 3 exposed by etching from p side nitride semiconductor layer side.

【０００８】

上記の如く、本発明の素子は、第１のｐ側窒化物半導体層のｐ側不純物の濃度に対し、ｐ側不純物濃度を少なく規定されたい第２のｐ側窒化物半導体層及びｐ側不純物濃度を多く規定された第３のｐ側窒化物半導体層を特定の積層順で形成することにより、発光素子出力を向上させることができる。即ち、コンタクト層として作用するｐ型不純物が高濃度にドープされた第３のｐ側窒化物半導体層と、その第３のｐ側窒化物半導体層より

[0008]

As mentioned above, the element of this invention, As opposed to the concentration of p side impurity of a first p side nitride semiconductor layer, the 2nd p side nitride semiconductor layer in which p side impurity concentration was stipulated few, and the third p side nitride semiconductor layer in which many p side impurity concentration was stipulated are formed in the order of a specific lamination. Thereby, light-emitting-element output can be improved.

That is, the third p side nitride semiconductor layer by which the p-type impurity effected as a contact layer was doped in high concentration, the 2nd p side nitride semiconductor layer in which the p-type impurity was doped fewer than

も活性層に接近した位置に、ｐ型不純物が第１のｐ側窒化物半導体層よりも少なくドープされた第２のｐ側窒化物半導体層、さらに第２の窒化物半導体よりも活性層に接近した位置にｐ型不純物が第３より少なく且つ第２より多くドープされた第１のｐ側窒化物半導体層とを備えることにより、素子全体の出力を向上させることができる。

a first p side nitride semiconductor layer by the position which approached the active layer from that third p side nitride semiconductor layer, Furthermore the first p side nitride semiconductor layer which the p-type impurity was doped fewer than the 3rd, and doped more than the 2nd by the position close to the active layer than the 2nd nitride semiconductor, the output of the entire element can be improved by providing an above.

【０００９】
活性層４は少なくともＩｎを含む窒化物半導体層を含む単一量子井戸構造、若しくは多重量子井戸構造とする。井戸層は膜厚１００オングストローム以下、さらに好ましくは７０オングストローム以下の$In_{X}Ga_{1-X}N$（０＜Ｘ≦１）で構成することが望ましく、また障壁層は井戸層よりもバンドギャップエネルギーが大きい$In_{Y}Al_{Z}Ga_{1-Y-Z}N$（０≦Ｙ、０≦Ｚ、Ｙ＋Ｚ≦１）を２００オングストローム以下、さらに好ましくは１５０オングストローム以下の膜厚で構成することが望ましい。

[0009]
An active layer 4 is taken as the single quantum well structure containing the nitride semiconductor layer which includes In at least, or the multiquantum well structure.

A well layer is 100 angstroms or less film thickness. It is preferable to comprise from InXGa1- XN (0<X=<1) 70 angstroms or less more preferably. Moreover a barrier layer, InYAlZGa1-Y- ZN (0=<Y, 0=<Z, Y+Z=<1) with a band-gap energy larger than a well layer is 200 angstroms or less. It is preferable to comprise from a film thickness 150 angstroms or less more preferably.

【００１０】
第１のｐ側窒化物半導体層５はｐ型不純物を含む窒化物半導体層で構成されていれば良く、特に活性層に接していてもいなくても良い。半導体としては活性層よりもバンドギャップエネルギーの大きい窒化物半導体を選択し、例えば前記のように$Al_{X}Ga_{1-X}N$（０≦Ｘ≦１）を好ましく成長させる。第１のｐ側窒化物半導体層５にドープするｐ

[0010]
The first p side nitride semiconductor layer 5 should just consist of the nitride semiconductor layer containing a p-type impurity.

Especially an active layer may be contacted. It does not need to contact.

The nitride semiconductor with a band-gap energy larger than an active layer as a semiconductor is selected.

For example, AlXGa1- XN (0=<X=<1) is grown preferably as mentioned above.

The p-type impurity concentrations doped in the first p side nitride semiconductor layer 5 are 1*1017/cm3 or more, and less than 1*1020/cm

型不純物濃度は、１×１０^{17}／cm^{3}以上、１×１０^{20}／cm^{3}以下、好ましくは１×１０^{18}／cm^{3}以上、より好ましくは１×１０^{19}／cm^{3}に調整する。但し、この範囲内において、第２の窒化物半導体層より多く且つ第３の窒化物半導体層より少なくなるよう調整される。ｐ型不純物濃度が上記範囲であると本発明の効果を得るのに好ましい。第１のｐ型窒化物半導体層５にドープすることのできるｐ型不純物としては、例えばＭｇ、Ｚｎ、Ｃｄ、Ｃａ、Ｂｅ、Ｓｒ等のII族元素を好ましくドープする。さらにこの第１の窒化物半導体層を互いに組成の異なる２種類の窒化物半導体層が積層されてなる超格子層とすることもできる。超格子層とする場合、超格子層を構成する窒化物半導体層の膜厚は１００オングストローム以下、さらに好ましくは７０オングストローム以下、最も好ましくは５０オングストローム以下の膜厚に調整する。膜厚がこの範囲であると発光出力及び順方向電圧の点で好ましい。また本発明において、第１の窒化物半導体層５を超格子層とすると、窒化物半導体層の結晶性が良くなり、出力がさらに向上する。超格子層とする場合、ｐ型不純物は両方の層にドープしても良いし、いずれか一方の層にドープしても良い。

3.

Preferably, 1*1018 / cm3 or more. It is 1*1019/cm3 more preferable. It adjusts in this way.

However, within the range of this, it adjusts so that it may more than 2nd nitride semiconductor layer and fewer than third nitride semiconductor layer.

When a p-type impurity concentration is the above range, it is preferable for obtaining the effect of this invention.

As the p-type impurity which can be doped in the first p-type nitride semiconductor layer 5, for example, II group elements, such as Mg, Zn, Cd, Ca, Be, and Sr, are doped preferably.

Furthermore also make this first nitride semiconductor layer be the superlattice layer which 2 kinds of nitride semiconductor layers from which a composition is mutually different are laminated, and turn into.

When doing as a superlattice layer, the film thickness of the nitride semiconductor layer which comprises a superlattice layer is 100 angstroms or less. More preferably, it is 70 angstroms or less. Most preferably, it is 50 angstroms or less. It adjusts to an above-mentioned film thickness.

When a film thickness is this range, it is preferable in points of light-emission output and a forward-direction voltage.

Moreover in this invention, if the first nitride semiconductor layer 5 is made into a superlattice layer, the crystallinity of a nitride semiconductor layer will become better.

Output improves further.

When doing as a superlattice layer, a p-type impurity may be doped in both of layers.

It may dope in any one layer.

【００１１】
第２の窒化物半導体層６は第１の窒化物半導体層５に接して形成されていることが望ましい

[0011]
2nd nitride semiconductor layer 6, although it is preferable to form in contact with the first nitride semiconductor layer 5, it does not need to

が、特に接して形成されていなくても良い。例えば第１と第２の窒化物半導体層との間に数百オングストローム以下の膜厚のアンドープの窒化物半導体層を成長させることもできる。第２の窒化物半導体層６にドープされるｐ型不純物は、第１及び第３の各窒化物半導体層５、６よりも少なくなるように調整することが望ましく、具体的には1×10^{20}／cm^3未満、好ましくは1×10^{19}／cm^3下、より好ましくは1×10^{18}／cm^3に調整する。また第２の窒化物半導体層は、不純物がドープされていなくてもよい。また、この範囲内において、第１及び第３の各窒化物半導体層より少なくなるよう調整される。ｐ型不純物濃度が上記範囲であると本発明の効果を得るのに好ましい。第２の窒化物半導体層にドープされるｐ型不純物は第１の窒化物半導体層にドープできる不純物と同様のものが挙げられる。第２の窒化物半導体層の組成は特に問うものではないが、好ましくは第３の窒化物半導体層と同一組成とする。第２の窒化物半導体層の膜厚は２μｍ以下、さらに好ましくは１μｍ以下、最も好ましくは０．５μｍ以下に調整する。膜厚がこの範囲であると発光出力及び順方向電圧の点で好ましい。また第２の窒化物半導体層を窒化物半導体の多層膜（超格子を含む）構造として、その多層膜を構成する窒化物半導体層のｐ型不純物濃度を段階的に少なくなるようにしても良い。

contact and form especially.

For example, the nitride semiconductor layer of the undoped of the film thickness below several hundred angstrom can also be grown between first and second nitride semiconductor layers.

As for the p-type impurity doped by the 2nd nitride semiconductor layer 6, it is preferable to adjust so that it may be fewer than the 1st and third of each nitride semiconductor layers 5 and 6. It is less than 1*1020/cm 3 specifically.

Preferably, it is under 1*1019 / cm3. It is 1*1018/cm3 more preferable. It adjusts in the above.

Moreover as for the 2nd nitride semiconductor layer, the impurity does not need to be doped.

Moreover, it adjusts so that it may be fewer than the 1st and third of each nitride semiconductor layer within the range of this.

When a p-type impurity concentration is the above range, it is preferable for obtaining the effect of this invention.

The p-type impurity doped by the 2nd nitride semiconductor layer, the similar thing as the impurity which can be doped in a first nitride semiconductor layer is mentioned.

Especially the composition of a 2nd nitride semiconductor layer does not ask.

However, preferably, it does as the same composition as a third nitride semiconductor layer.

The film thickness of a 2nd nitride semiconductor layer is 2 μm or less. More preferably, it is 1 μm or less. Most preferably, it is below 0.5 μm. It adjusts in the above.

When a film thickness is this range, it is preferable in points of light-emission output and a forward-direction voltage.

Moreover a 2nd nitride semiconductor layer is made into the multilayer film (superlattice is included) structure of a nitride semiconductor. It may be made to decrease the p-type impurity concentration of the nitride semiconductor layer which comprises that multilayer film stepwise.

【0012】
第3の窒化物半導体層7は、p電極を形成するコンタクト層とすることが望ましく、好ましくはX値が0.3以下の$Al_xGa_{1-x}N$（0≦X≦0．3）とするとp電極と好ましいオーミックが得られる。第3の窒化物半導体層7のp型不純物濃度は、1×10^{18}／cm^3以上、1×10^{21}／cm^3以下、好ましくは1×10^{19}／cm^3以上、より好ましくは2×10^{20}／cm^3に調整することが望ましい。またこの範囲内において、第1及び第2の各窒化物半導体層より多くなるよう調整される。p型不純物濃度が上記範囲であると本発明の効果を得るのに好ましい。また第3の窒化物半導体層の膜厚は第2の窒化物半導体層よりも薄く調整することが望ましい。即ち、コンタクト層として作用する第3のp型窒化物半導体層の膜厚を薄くして、高濃度にp型不純物をドープすることによりコンタクト抵抗が下がるので、Ｖｆ（順方向電圧）が低下しやすい傾向にある。第3の窒化物半導体層の膜厚として具体的には、1μm以下、さらに好ましくは0．1μm以下、最も好ましくは0．05μm以下に調整する。膜厚がこの範囲であると発光出力及び順方向電圧の点で好ましい。

[0012]
As for the third nitride semiconductor layer 7, it is preferable to do as the contact layer which forms p electrode. Preferably if X value considers as 0.3 or less AlXGa1- XN (0=<X=<0.3), p electrode and a preferable ohmic will be obtained.
The p-type impurity concentrations of the third nitride semiconductor layer 7 are 1*1018 / cm3 or more, and less than 1*1021/cm3.
Preferably, they are 1*1019 / cm3 or more. It is 2*1020/cm3 more preferable. Adjusting in the above is preferable.
Moreover it adjusts so that it may increase more than each first and second nitride semiconductor layer within the range of this.
When a p-type impurity concentration is in the above range, it is preferable for obtaining the effect of this invention.
Moreover as for the film thickness of a third nitride semiconductor layer, it is preferable to adjust thinner than a 2nd nitride semiconductor layer.
That is, the film thickness of the third p-type nitride semiconductor layer effected as a contact layer is made thin.
A p-type impurity is doped in high concentration. Because a contact resistance accordingly falls, it is in the tendency that Vf (forward-direction voltage) tends to reduce.
As the film thickness of a third nitride semiconductor layer, Specifically, it is 1 μm or less. More preferably, it is 0.1 μm or less. Most preferably, it adjusts to 0.05 μm or less.
When a film thickness is in this range, it is preferable in points of light-emission output and a forward-direction voltage.

【0013】
また、本発明の窒化物半導体素子を構成するのその他の構成は、特に限定されず、少なくと

[0013]
Moreover, other component of comprising the nitride semiconductor element of this invention is not limited especially. What is sufficient is just

も上記本発明の構成を満たす物であればよい。

to be the object which satisfies the component of above this invention at least.

【００１４】

[0014]

【実施例】
以下、本発明の実施例を示すが、本発明はこれに限定されない。本発明の実施例において、窒化物半導体素子はＭＯＣＶＤ法を用いて製造される。

[Example]
Hereafter, the example of this invention is shown.
However, this invention is not limited to this.
In the example of this invention, a nitride semiconductor element is manufactured using MOCVD method.

【００１５】

[0015]

【実施例１】
サファイア（０００１）面を主面とする基板を用意し、原料ガスにＴＭＧ（トリメチルガリウム）、アンモニアを用いて５００℃でＧａＮよりなるバッファ層を２００オングストロームの膜厚で成長させる。

[Example 1]
The substrate which makes a sapphire (0001) surface a main surface is prepared.
TMG (trimethyl gallium) and ammonia are used for starting-material gas, and the buffer layer which consists of GaN at 500 degree C is grown by the 200 angstroms film thickness.

【００１６】
次に温度を１０５０℃に上昇させ、ＴＭＧ、アンモニア、不純物ガスにモノシランガスを用いて、Ｓｉを$1\times10^{19}/cm^3$ドープしたｎ型ＧａＮ層を５μｍの膜厚で成長させる。

[0016]
Next temperature is risen at 1050 degree C.
Monosilane gas is used for TMG, ammonia, and impurity gas.
The n-type GaN layer which doped Si 1*1019/cm3 is grown by the 5-μm film thickness.

【００１７】
次に温度を８００℃にして、ＴＭＩ（トリメチルインジウム）、ＴＭＧ、アンモニアを用い、活性層として、アンドープ$In_{0.4}Ga_{0.6}N$よりなる井戸層を２５オングストロームの膜厚で成長させる。

[0017]
Next temperature is made into 800 degree C.
TMI (trimethyl indium), TMG, and ammonia are used. As an active layer, the well layer which consists of undoped In0.4Ga0.6N is grown by the 25 angstroms film thickness.

【００１８】

[0018]

次に温度を１０５０℃にして、ＴＭＧ、アンモニア、不純物ガスとしてＣp_2Ｍｇ（シクロペンタジエニルマグネシウム）を用い、Ｍｇを１×１０^{19}／cm^{3}ドープしたｐ型Ａｌ$_{0.3}$Ｇａ$_{0.7}$Ｎよりなる第１の窒化物半導体層を２００オングストロームの膜厚で成長させる。この第１の窒化物半導体層はキャリアを閉じ込める層として作用する。

Next temperature is made into 1050 degree C.
TMG, ammonia, and cp2 mg (cyclopentadienyl magnesium) as impurity gas is used. The first nitride semiconductor layer which consists of p-type Al0.3Ga0.7N which doped Mg 1*1019/cm3 is grown by the 200 angstroms film thickness.
This first nitride semiconductor layer is effected as a layer which locks up a carrier.

【００１９】

第１の窒化物半導体層成長後、原料ガスを止め、続いて再度ＴＭＧ、アンモニア、Ｃp_2Ｍｇを流し、１０５０℃で、Ｍｇを１×１０^{18}／cm^{3}ドープしたＧａＮよりなる第２の窒化物半導体層を０．１８μｍの膜厚で成長させる。

[0019]

Starting-material gas is stopped after first nitride semiconductor layer-formation length.
Subsequently TMG, ammonia, and Cp2 mg are poured again.
The 2nd nitride semiconductor layer which consists of GaN which doped Mg 1*1018/cm3, at 1050 degree C is grown by the 0.18-μm film thickness.

【００２０】

第２の窒化物半導体層成長後、ＴＭＧ、アンモニア、Ｃp_2Ｍｇを用い、Ｍｇを２×１０^{20}／cm^{3}ドープした第３の窒化物半導体層を３００オングストロームの膜厚で成長させる。

[0020]

After 2nd nitride semiconductor layer-formation length, the third nitride semiconductor layer which doped Mg 2*1020/cm3 is grown by the 300 angstroms film thickness using TMG, ammonia, and Cp2 mg.

【００２１】

以上のようにして窒化物半導体を成長させたウェーハを反応容器内において、窒素雰囲気中７００℃でアニーリングを行い、ｐ型不純物をドープした層をさらに低抵抗化させる。アニーリング後、ウェーハを反応容器から取り出し、ＲＩＥ装置により最上層の第３の窒化物半導体層側からエッチングを行い、ｎ電極を形成すべきｎ側コンタクト

[0021]

The wafer which grew the nitride semiconductor as mentioned above, An annealing is performed at 700 degree C in nitrogen atmosphere in the reaction container.
The layer which doped the p-type impurity is made to form into a low resistance further.
A wafer is picked out from the reaction container after an annealing.
RIE device performs an etching from the third nitride semiconductor layer side of uppermost layer.
The surface of n side contact layer which should form n electrode is exposed.

層の表面を露出させる。最上層の第３の窒化物半導体層のほぼ全面にＮｉ／Ａｕよりなる全面電極を２００オングストロームの膜厚で形成し、その全面電極の一部に１μｍの膜厚でＡｕよりなるパッド電極を形成する。一方、露出させたｎ側コンタクト層の表面には、ＷとＡｕよりなるｎ電極を形成する。

The whole-surface electrode of the third nitride semiconductor layer of uppermost layer which consists of Ni/Au almost entirely is formed by the 200 angstroms film thickness.

The pad electrode comprising Au is formed by the 1-μm film thickness in a part of that whole-surface electrode.

On the other hand, n electrode which consists of W and Au is formed in the surface of exposed n side contact layer.

【００２２】

以上のようにして電極を形成したウェーハを３５０μｍ角のチップに分離し、発光させたところ２０ｍＡにおいて、Ｖｆ３．２Ｖ、発光波長５２５ｎｍ、光出力３．５ｍＷ、外部量子効率７．３％となり、従来の緑色ＬＥＤに比較して、およそ１．３倍に向上した。

[0022]

As mentioned above, the wafer which formed the electrode was made to isolate to the chip of 350 μm angle and emit light. In 20mA, it becomes Vf3.2V, the light-emission wavelength of 525 nm, 3.5 mW of optical powers, and 7.3% of external quantum efficiencies.

Compared with the conventional green LED, it improved by about 1.3 times.

【００２３】

[0023]

【実施例２】

実施例１において、第１の窒化物半導体層にＭｇを5×10^{19}/cm^{3}ドープし、第２の窒化物半導体層にＭｇを5×10^{17}/cm^{3}ドープし、第３の窒化物半導体層にＭｇを1×10^{20}/cm^{3}ドープし、その他は同様にして行ったところ、実施例１とほぼ同様な特性を有するＬＥＤ素子を得ることができた。

[Example 2]

In an example 1, Mg is doped 5*1019/cm3 in a first nitride semiconductor layer.

Mg is doped 5*1017/cm3 in a 2nd nitride semiconductor layer. Mg is doped 1*1020/cm3 in a third nitride semiconductor layer. When others were performed similarly, they were able to obtain LED element which has the almost similar property as an example 1.

【００２４】

[0024]

【実施例３】

図２は本発明に係る一レーザ素

[Example 3]

Fig. 2 is a model sectional view showing the structure of the one laser element based on this

子の構造を示す模式的な断面図であり、以下、この図を元に本発明の第３実施例について説明する。

invention.

Hereafter, this diagram is explained to an element about the 3rd example of this invention.

【００２５】
サファイア（０００１）面を主面とする基板の上にＧａＮよりなるバッファ層を介してＧａＮよりなる単結晶を１２０μｍの膜厚で成長させたＧａＮ基板１００を用意する。このＧａＮ基板１００をサファイアの上に成長させた状態で、反応容器内にセットし、温度を１０５０℃まで上げ、実施例１と同様にして、ＧａＮ基板１００上にＳｉを１×１０^{18}／cm^{3}ドープしたＧａＮよりなるｎ側バッファ層１１を４μｍの膜厚で成長させる。このｎ側バッファ層は高温で成長させるバッファ層であり、例えば実施例１のように、サファイア、ＳｉＣ、スピネルのように窒化物半導体と異なる材料よりなる基板の上に、９００℃以下の低温において、ＧａＮ、ＡｌＮ等を、０．５μｍ以下の膜厚で直接成長させるバッファ層２とは区別される。

[0025]
On the substrate which makes a sapphire (0001) surface a main surface, the GaN substrate 100 which grew the single crystal which consists of GaN, by the 120-μm film thickness via the buffer layer which consists of GaN is prepared.
In the condition of having made it growing on sapphire, this GaN substrate 100 is set in the reaction container.

Temperature is raised to 1050 degree C and it is made to be the same as that of an example 1.

n side buffer layer 11 which consists of GaN which doped Si 1*1018/cm3 on the GaN substrate 100 is grown by the 4-μm film thickness.

This n side buffer layer is a buffer layer grown at high temperature.

For example, the buffer layer 2 which grows GaN and AlN etc. into 900 degree C or less low temperature directly by the film thickness below 0.5 μm on the substrate which consists of the material which is different from a nitride semiconductor such as sapphire, SiC, and a spinel, such as an example 1 is distinguished.

【００２６】
（ｎ側クラッド層１２＝歪み超格子層）続いて、１０５０℃でＴＭＡ（トリメチルアルミニウム）、ＴＭＧ、アンモニア、シランガスを用い、Ｓｉを１×１０^{19}／cm^{3}ドープしたｎ型Ａｌ$_{0.3}$Ｇａ$_{0.7}$Ｎよりなる第１の層を４０オングストロームの膜厚で成長させ、続いてシランガス、ＴＭＡを止め、アンドープのＧ

[0026]
(n side clad layer 12= distortion super-latticed layer) Subsequently, TMA (trimethylaluminum), TMG, ammonia, and silane gas are used at 1050 degree C. The first layer which consists of n-type Al0.3Ga0.7N which doped Si 1*1019/cm3 is grown by the 40 angstroms film thickness.

Subsequently silane gas and TMA are stopped and the 2nd layer which consists of GaN of an undoped is grown by the 40 angstroms film thickness.

ａＮよりなる第２の層を４０オングストロームの膜厚で成長させる。そして第１層＋第２層＋第１層＋第２層＋・・・というように歪み超格子層を構成し、それぞれ１００層ずつ交互に積層し、総膜厚０．８μｍの歪み超格子よりなるｎ側クラッド層１２を成長させる。

And the distortion super-latticed layer is comprised like 1st-layer + 2nd layer + 1st-layer + 2nd layer +***.
It respectively laminates 100 layers at a time alternately.
n side clad layer 12 which consists of the strained super lattice of the 0.8 μm of the total film thickness is grown.

【００２７】
（ｎ側光ガイド層１３）続いて、シランガスを止め、１０５０℃でアンドープＧａＮよりなるｎ側光ガイド層１３を０．１μｍの膜厚で成長させる。このｎ側光ガイド層は、活性層の光ガイド層として作用し、ＧａＮ、ＩｎＧａＮを成長させることが望ましく、通常１００オングストローム～５μｍ、さらに好ましくは２００オングストローム～１μｍの膜厚で成長させることが望ましい。またこの層をアンドープの歪み超格子層とすることもできる。歪み超格子層とする場合にはバンドギャップエネルギーは活性層より大きく、ｎ側クラッド層よりも小さくする。

[0027]
(n side light-guide layer 13) Subsequently, silane gas is stopped.
n side light-guide layer 13 which consists of a undoped GaN at 1050 degree C is grown by the 0.1-μm film thickness.
As for this n side light-guide layer, it is preferable to effect as a light-guide layer of an active layer, and to grow GaN and InGaN. Usually 100 angstroms - 5 μm, It is preferable to make it grow by the 200 angstroms - 1 μm film thickness more preferably.
Moreover also make this layer be the strained-super-lattice layer of an undoped.
When doing as the distortion super-latticed layer, a band-gap energy is larger than an active layer, and is made smaller than n side clad layer.

【００２８】
（活性層１４）次に、原料ガスにＴＭＧ、ＴＭＩ、アンモニアを用いて活性層１４を成長させる。活性層１４は温度を８００℃に保持して、アンドープ$Ｉｎ_{0.2}Ｇａ_{0.8}Ｎ$よりなる井戸層を２５オングストロームの膜厚で成長させる。次にＴＭＩのモル比を変化させるのみで同一温度で、アンドープ$Ｉｎ_{0.01}Ｇａ_{0.95}$

[0028]
(Active layer 14) Next, TMG, TMI, and ammonia are used for starting-material gas, and an active layer 14 is grown.
An active layer 14 maintains temperature at 800 degree C.
The well layer which consists of undoped In0.2Ga0.8N is grown by the 25 angstroms film thickness.
Next the barrier layer which consists of undoped In0.01Ga0.95N at the same temperature only by changing molar ratio of TMI

Ｎよりなる障壁層を５０オングストロームの膜厚で成長させる。この操作を２回繰り返し、最後に井戸層を積層した総膜厚１７５オングストロームの多重量子井戸構造（ＭＱＷ）の活性層を成長させる。活性層は本実施例のようにアンドープでもよいし、またｎ型不純物及び／又はｐ型不純物をドープしても良い。不純物は井戸層、障壁層両方にドープしても良く、いずれか一方にドープしてもよい。

is grown by the 50 angstroms film thickness.

This operation is repeated twice and the active layer of the multiquantum well structure (MQW) of the 175 angstroms of the total film thickness which finally laminated the well layer is grown.

An undoped is suitable as an active layer such as this example.

Moreover an n-type impurity and/or a p-type impurity may be doped.

An impurity may be doped to both well layer and barrier layer, and may be doped to any one.

【００２９】

（ｐ側キャップ層１５）次に、温度を１０５０℃に上げ、ＴＭＧ、ＴＭＡ、アンモニア、Cp_2Mg（シクロペンタジエニルマグネシウム）を用い、ｐ側光ガイド層１６よりもバンドギャップエネルギーが大きい、Ｍｇを$1\times10^{19}/cm^3$ドープしたｐ型$Al_{0.3}Ga_{0.7}N$よりなるｐ側キャップ層１７を３００オングストロームの膜厚で成長させる。ｐ側キャップ層は０．５μｍ以下、さらに好ましくは０．１μｍ以下の膜厚で成長させると、ｐ側キャップ層がキャリアを活性層内に閉じ込めるためのバリアとして作用するので、出力が向上する。このｐ型キャップ層１５の膜厚の下限は特に限定しないが、１０オングストローム以上の膜厚で形成することが望ましい。

[0029] 15

(p side cap layer 15) Next, temperature is raised to 1050 degree C and TMG, TMA, ammonia, and Cp2 mg (cyclopentadienyl magnesium) are used. p side cap layer ~~17~~ which consists of p-type Al0.3Ga0.7N to which the band-gap energy doped large Mg 1*1019/cm3 from p side light-guide layer 16 is grown by the 300 angstroms film thickness.

p side cap layer is below 0.5 μm. More preferably, it is 0.1 μm or less. If it is made to grow by the above-mentioned film thickness, because it will effect as a barrier for p side cap layer locking up a carrier in an active layer, output improves.

Especially the lower limit of the film thickness of this p-type cap layer 15 does not limit.

However, it is preferable to form by the film thickness 10 angstroms or more.

【００３０】

（ｐ側光ガイド層１６）ｐ側キャップ層１５成長後、再度ＴＭＧ、Cp_2Mg、アンモニアを用

[0030]

(p side light-guide layer 16) It is again made to be the same as that of an example 1 after the p side cap layer 15 growth using TMG, Cp2 mg,

い、実施例１と同様にして、１０５０℃で、バンドギャップエネルギーがｐ側キャップ層１５よりも小さい、Ｍｇを１×１０^{20}／cm^{3}ドープしたＧａＮよりなるｐ側光ガイド層１６を０．１μｍの膜厚で成長させる。この層は、活性層の光ガイド層として作用する。

and ammonia.
p side light-guide layer 16 which consists of GaN to which the band-gap energy doped Mg smaller than p side cap layer 15 1*1020/cm3, at 1050 degree C is grown by the 0.1-μm film thickness.
This layer is effected as a light-guide layer of an active layer.

【００３１】
（ｐ側クラッド層１７＝第１の窒化物半導体層）続いて、１０５０℃でＭｇを１×１０^{20}／cm^{3}ドープしたｐ型Ａｌ$_{0.3}$Ｇａ$_{0.8}$Ｎよりなる層を４０オングストロームの膜厚で成長させ、続いてＴＭＡのみを止め、Ｍｇを１×１０^{19}／cm^{3}ドープしたｐ型ＧａＮよりなる層を４０オングストロームの膜厚で成長させる。そしてこの操作をそれぞれ１００回繰り返し、総膜厚０．８μｍの歪み超格子層よりなるｐ側クラッド層１７を形成する。ｐ側クラッド層のＭｇの平均濃度は、５×１０^{19}／cm^{3}である。

[0031]
(p side clad layer 17= first nitride semiconductor layer) Subsequently, the layer comprising p-type Al0.3Ga0.8N which doped Mg 1*1020/cm3 at 1050 degree C is grown by the 40 angstroms film thickness.
Subsequently only TMA is stopped and the layer which consists of the p-type GaN which doped Mg 1*1019/cm3 is grown by the 40 angstroms film thickness.
And this operation is respectively repeated 100 times.
p side clad layer 17 which consists of the strained-super-lattice layer of the 0.8 μm of the total film thickness is formed. ,8μ
The equilibrium concentration of Mg of p side clad layer is 5*1019/cm3.

【００３２】
（ｐ側コンタクト層１８＝第２及び第３の窒化物半導体層）最後に、１０５０℃で、ｐ側クラッド層１７の上に、Ｍｇを１×１０^{18}／cm^{3}ドープしたｐ型ＧａＮよりなる層（第２の窒化物半導体層）を０．１μｍの膜厚で成長させ、続いてＭｇを２×１０^{20}／cm^{3}ドープしたｐ型ＧａＮよりなる層（第３の窒化物半導体層）を２００オングストロームの膜厚で成長させる。ｐ

[0032]
(p side contact layer 18= the 2nd and third nitride semiconductor layer) Finally the layer (2nd nitride semiconductor layer) which consists of the p-type GaN which doped Mg 1*1018/cm3 on p side clad layer 17, at 1050 degree C is grown by the 0.1-μm film thickness.
Subsequently the layer (third nitride semiconductor layer) which consists of the p-type GaN which doped Mg 2*1020/cm3 is grown by the 200 angstroms film thickness.
p side contact layer 18 can consist of InXAlYGa1-X- YN (0=<X, 0=<Y, X+Y=<1) of a p-type.
If it makes GaN which preferably doped Mg,

側コンタクト層１８はｐ型のＩｎ$_X$Ａｌ$_Y$Ｇａ$_{1\text{-}X\text{-}Y}$Ｎ（０≦X、０≦Y、X+Y≦１）で構成することができ、好ましくはＭｇをドープしたＧａＮとすれば、ｐ電極２１と最も好ましいオーミック接触が得られる。またｐ型Ａｌ$_Y$Ｇａ$_{1\text{-}Y}$Ｎを含む歪み超格子構造のｐ側クラッド層１７に接して、バンドギャップエネルギーの小さい窒化物半導体をｐ側コンタクト層として、その膜厚を５００オングストローム以下と薄くしているために、実質的にｐ側コンタクト層１８のキャリア濃度が高くなりｐ電極と好ましいオーミックが得られて、素子の閾値電流、電圧が低下する。

most preferable ohmic contact as the p electrode 21 will be obtained.
p side clad layer 17 of the distortion superstructure which includes p-type AlYGa1-YN also is contacted.

Make the small nitride semiconductor of a band-gap energy be p side contact layer. That film thickness is made thin with 500 angstroms or less. Therefore, the carrier concentration of p side contact layer 18 becomes high substantially, and an ohmic as preferable as p electrode is obtained.

The threshold-value current of an element and a voltage reduce.

【００３３】
以上のようにして窒化物半導体を成長させたウェーハを反応容器内において、窒素雰囲気中７００℃でアニーリングを行い、ｐ型不純物をドープした層をさらに低抵抗化させる。

[0033]
An annealing is performed the wafer which grew the nitride semiconductor as mentioned above, at 700 degree C in nitrogen atmosphere in the reaction container.

The layer which doped the p-type impurity is made to form into a low resistance further.

【００３４】
アニーリング後、ウェーハを反応容器から取り出し、図３に示すように、ＲＩＥ装置により最上層のｐ側コンタクト層１８と、ｐ側クラッド層１７とをエッチングして、４μｍのストライプ幅を有するリッジ形状とする。このように、活性層よりも上部にある層をストライプ状のリッジ形状とすることにより、活性層の発光がストライプリッジの下に集中するようになって閾値が低下する。特に歪み超格

[0034]
A wafer is picked out from the reaction container after an annealing.
As shown in Fig. 3, p side contact layer 18 of uppermost layer and p side clad layer 17 are etched with RIE device.

It considers as the ridge shape where it has the stripe width of 4 μm.

Thus, by making the layer which exists above an active layer into a stripe-like ridge shape, a light emission of an active layer comes to concentrate on the bottom of a stripe ridge, and a threshold-value reduces.

It is preferable to make the layer of 17 or more of p side clad layers which consist especially of the distortion super-latticed layer

子層よりなるｐ側クラッド層１７以上の層をリッジ形状とすることが好ましい。

into a ridge shape.

【００３５】

リッジ形成後、ｐ側コンタクト層１８のリッジ最表面にＮｉ／Ａｕよりなるｐ電極２１をストライプ状に形成し、ｐ電極２１以外の最表面の窒化物半導体層のにＳｉO_2よりなる絶縁膜２５を形成し、この絶縁膜２５を介してｐ電極２１と電気的に接続したｐパッド電極２２を形成する。

[0035]

The p electrode 21 comprising Ni/Au is formed in the ridge outermost surface of p side contact layer 18 stripe-like after ridge formation.

The insulating film 25 comprising SiO2 is formed in the nitride semiconductor layer of outermost surfaces except for p electrode 21.

p pad electrode 22 which connected with the p electrode 21 electrically via this insulating film 25 is formed.

【００３６】

以上のようにして、ｐ電極を形成したウェーハを研磨装置に移送し、サファイア基板を研磨により除去し、ＧａＮ基板１０の表面を露出させる。露出したＧａＮ基板表面のほぼ全面にＴｉ／Ａｌよりなるｎ電極２３を形成する。

[0036]

The wafer which formed p electrode as mentioned above is transferred to a polish device.

A sapphire substrate is removed by the polishing.

The surface of the GaN substrate 10 is exposed.

The n electrode 23 of exposed GaN substrate surface which consists of Ti/Al almost entirely is formed.

【００３７】

電極形成後ＧａＮ基板のＭ面（窒化物半導体を六方晶系で近似した場合に六角柱の側面に相当する面）で劈開し、その劈開面にＳｉO_2とＴｉO_2よりなる誘電体多層膜を形成し、最後にｐ電極に平行な方向で、バーを切断してレーザ素子とする。

[0037]

It cleaves by M coats (surface which is equivalent to the side of a hexagonal column when approximating a nitride semiconductor by the hexagonal system) of GaN substrate after electrode formation.

The dielectric multilayer film which becomes that cleavage plane from SiO2 and TiO2 is formed, and finally, in a direction parallel to p electrode, a bar is cut and it considers as a laser element.

【００３８】

このレーザチップをフェースアップ（基板とヒートシンクとが対向した状態）でヒートシンクに設置し、それぞれの電極をワ

[0038]

This laser chip is installed to a heat sink by face up (condition which the substrate and the heat sink oppositely faced), and the wire bonding of each electrode is performed.

イヤーボンディングして、室温でレーザ発振を試みたところ、室温において、閾値電流密度２．０ｋＡ／cm^2、閾値電圧４．０Ｖで、発振波長４０５ｎｍの連続発振が確認され、１０００時間以上の寿命を示した。

When attempting a laser oscillation at a room temperature, in a room temperature, A continuous oscillation with an oscillation wavelength of 405 nm is confirmed by 2.0kA/cm-squared threshold-value current density and threshold-voltage 4.0V.

Or more of the durability was shown for 1000 hours.

【００３９】

[0039]

【発明の効果】

このように、本発明の窒化物半導体素子では、活性層の上に積層される複数の窒化物半導体層のｐ型不純物の濃度を特定の範囲に規定し且つ積層順を特定することにより、出力を大幅に向上させることができる。また本発明の素子はＬＥＤ、ＬＤのような発光デバイスだけではなく、他の受光デバイスのような窒化物半導体を用いた多くの電子デバイスに用いることができる。

[EFFECT OF THE INVENTION]

Thus, in the nitride semiconductor element of this invention, output can be greatly improved by stipulating the concentration of the p-type impurity of several nitride semiconductor layer laminated on an active layer in the specific range, and specifying the order of a lamination.

Moreover the element of this invention can be used not only for the light-emission device such as LED and LD but for many electronic device using the nitride semiconductor such as the other light-receiving device.

【図面の簡単な説明】

[BRIEF EXPLANATION OF DRAWINGS]

【図１】

本発明の一実施例に係るＬＥＤ素子の構造を示す模式断面図である。

[FIGURE 1]

It is the model sectional view showing the structure of LED element based on one example of this invention.

【図２】

本発明の他の実施例に係るＬＤ素子の構造を示す模式断面図である。

[FIGURE 2]

It is the model sectional view showing the structure of LD element based on the other example of this invention.

【符号の説明】

１・・・基板

２・・・バッファ層

３・・・ｎ側コンタクト層

[EXPLANATION OF DRAWING]

1*** substrate

2*** buffer layer

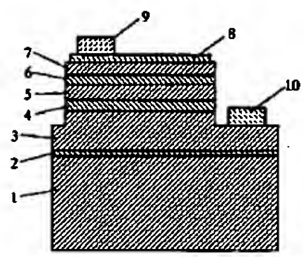
3***n side contact layer

4・・・活性層
5・・・第１のｐ側窒化物半導体層
6・・・第２のｐ側窒化物半導体層
7・・・第３のｐ側窒化物半導体層
8・・・ｐ電極
9・・・パッド電極
１０・・・ｎ電極

4*** active layer
5*** first p side nitride semiconductor layer
6*** 2nd p side nitride semiconductor layer
7*** third p side nitride semiconductor layer
8***p electrode
9*** pad electrode
10***n electrode

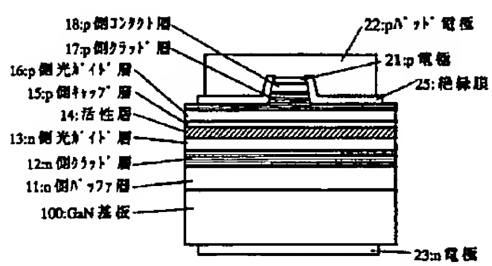
【図１】

[FIGURE 1]



【図２】

[FIGURE 2]



18: p side contact layer 17: p side clad layer 16: p side light-guide layer 15: p side cap layer 14: active layer 13: n side light-guide layer 12: n side clad layer 11: n side buffer layer 100: GaN substrate 22: p pad electrode 21: p electrode 25: insulating film 23: n electrode